Interview Summary	Application No.	Applicant(s)	
	09/552,383	WILLIS, STEPHEN L.	
	Examiner	Art Unit	
	José R Díaz	2815	

All participants (applicant, applicant's representative, PTO personnel):

(1) *José R Díaz*.

(2) *Eddie Lee*.

(3) *Michael Trenholm*.

(4) _____.

Date of Interview: *11 July 2003*.

Type: a)☐ Telephonic b)☐ Video Conference
c)☒ Personal [copy given to: 1)☐ applicant 2)☒ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *30 and 56*.

Identification of prior art discussed: *Shue (US 6,281,127 B1) and Sandhu et al. (US 5,069,002)*.

Agreement with respect to the claims f)☐ was reached. g)☒ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *Discussion focused over the prior art presented in the last Office action. Claim language was suggested. However, such claim language and arguments will be fully considered when file as a response to the last Office action.*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN ONE MONTH FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

7/11/03

Examiner's signature, if required

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

30 (Proposed). A method of forming a dielectric layer of a first thickness on a semiconductor wafer comprising:

forming the dielectric layer of the first thickness on the wafer;

positioning a shield layer on the dielectric layer;

positioning a sacrificial layer on the shield layer;

removing the conductive material and the sacrificial layer using a chemical mechanical polishing process adapted to remove the conductive material and the sacrificial layer until the shield layer is reached, wherein the shield layer is more resistant to planarization by the chemical mechanical polishing process than the sacrificial layer and wherein the shield layer inhibits thinning of the dielectric layer during the chemical mechanical polishing and wherein interposing the sacrificial layer between the conductive material and the shield layer reduces the amount of conductive material on the shield layer following the chemical mechanical polishing process; and

detecting when the chemical mechanical polishing has removed the sacrificial layer and halting the chemical mechanical process upon detecting when the sacrificial layer has been removed so as to maintain the dielectric layer at the first thickness.